

Status of Claims

Claims 1-9 (cancelled).

5 10. (Previously Amended) A method of creating a substrate having multiple regions for creating low-voltage transistors of a first and second conductivity and high-voltage transistors of a first conductivity, consisting essentially of the steps of:

10 creating a defined deposition of a first dielectric layer to expose a first region and a second region;
 implanting a first conductivity dopant into the first and second regions;
 applying a first protective coating over the first and second regions;
 driving in the first conductivity dopant into the substrate;
 removing the first dielectric layer;
15 creating a defined deposition of a second dielectric layer in the same location as the defined deposition of the first dielectric layer;
 implanting a second conductivity dopant in the substrate disposed under the defined deposition of the second dielectric layer;
 driving in the second conductivity dopant into the substrate;
20 removing the first protective coating and the second dielectric layer;
 creating a patterned third dielectric layer over the surface of the substrate to expose the drain and source of the first and second conductivity low-voltage transistors and the first conductivity high-voltage transistor;
 creating a defined deposition of a fourth dielectric layer disposed on the
25 drain and source of the first conductivity low-voltage transistor;
 applying a second protective coating over the first and second regions;
 implanting a second conductivity dopant into the substrate disposed under the drain and source of the first conductivity low-voltage transistor;
 removing the second protective coating;
30 creating a fifth dielectric layer in areas of the substrate where the third dielectric layer is not located;
 removing the patterned third dielectric layer; and
 then further comprising the steps of:

30 creating a sixth dielectric layer over the surface of the substrate to form a gate oxide;
 depositing a gate material over the sixth dielectric layer; and
 patterning the sixth dielectric layer and the gate material to define gate
 5 regions of the first and second low conductivity transistors and a gate region of the first conductivity high-voltage transistor.

Claim 11 (cancelled).

10 12. (Currently Amended) A method of creating an integrated circuit having a second conductivity type low-voltage ^{PMOS} transistor in a first region, a first conductivity type high-voltage ^{NMOS} transistor in a second region, and a first conductivity low-voltage transistor in a third region, comprising the steps of:

15 ^{B Int} doping the first and second regions with a first dopant concentration to both control the threshold voltage of the second conductivity type low-voltage transistor and set a breakdown voltage of the first conductivity high-voltage transistor; and

doping the third region with a second dopant concentration to control the threshold voltage of the first conductivity type low-voltage transistor;

20 wherein an additional voltage threshold adjust implant step to adjust the threshold voltages of the first and second low-voltage transistors is not performed.

Claim 13 (cancelled).

25 14. (Currently Amended) A method of processing an integrated circuit having a second conductivity type low-voltage transistor in a first region, a first conductivity high-voltage transistor in a third region, and a first conductivity low-voltage type transistor in a second region, comprising the steps of:

30 doping the first and second regions with a first dopant concentration thereby determining a threshold voltage of the second conductivity type low-voltage transistor and a breakdown voltage of the first conductivity type high-voltage transistor; and

doping the third region with a second dopant concentration; and
 excluding the step of:

implanting an additional threshold voltage adjustment of the first and second low-voltage transistors; and

wherein the first and second regions have the substantially the same dopant concentration after processing of the integrated circuit.

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Claim 15 (cancelled).

16. (Original) A method of creating a substrate having multiple regions for creating low-voltage transistors of a first and second conductivity and high-voltage transistors of a first conductivity, comprising the steps of:

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creating a defined deposition of a first dielectric layer to expose a first region and a second region; then

implanting a first conductivity dopant into the first and second regions; then
applying a first protective coating over the first and second regions; then
driving in the first conductivity dopant into the substrate; then
removing the first dielectric layer; then

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creating a defined deposition of a second dielectric layer in the same location as the defined deposition of the first dielectric layer; then

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implanting a second conductivity dopant in the substrate disposed under the defined deposition of the second dielectric layer; then

driving in the second conductivity dopant into the substrate; then
removing the first protective coating and the second dielectric layer; then
creating a patterned third dielectric layer over the surface of the substrate

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to expose the drain and source of the first and second conductivity low-voltage transistors and the first conductivity high-voltage transistor; then

creating a defined deposition of a fourth dielectric layer disposed on the drain and source of the first conductivity low-voltage transistor; then

applying a second protective coating over the first and second regions;
then

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implanting a second conductivity dopant into the substrate disposed under the drain and source of the first conductivity low-voltage transistor; then

removing the second protective coating; then

creating a fifth dielectric layer in areas of the substrate where the third dielectric layer is not located; then

removing the patterned third dielectric layer;
creating a sixth dielectric layer over the surface of the substrate to form a
gate oxide;
depositing a gate material over the sixth dielectric layer; and
5 patterning the sixth dielectric layer and the gate material to define gate
regions of the first and second low conductivity transistors and a gate region of the
first conductivity high-voltage transistor.

Claim 17 (cancelled).

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